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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,964	12/19/2001	Kyujin Jung	4459-014A	1168

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,964	JUNG ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-9,14-18 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-9,14-18 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/03/2004 has been entered. A new rejection is made as set forth in this Office Action. Claims (5-9, 14-18, and 21-25) are pending in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 5, 6, 9, and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coffman (U.S. Patent 6,451,627) in view of Yoneda et al. (U.S. Pub. 2002/0027265).

In re claims 5, 6 and 9, **Coffman** disclose a method of making a low-pin-count chip package, the method comprising the steps of (**FIGS. 1-17** and related text): providing a sheet carrier **(FIG. 12: 126)**; laminating a metal layer **(FIG. 12: 124)** on the sheet carrier; half-etching the metal layer so as to form cavities **(FIG. 14: 142)** at the predetermined positions thereof (col. 5, line 56 to col. 6, line 13 and **FIG. 14**); forming a photoresist layer **(FIG. 3: 32)** on the half-etched metal layer (col. 2, line 59 to col. 3, line

20); half-removing the photoresist layer such that only the photoresist within the cavities is left (col. 2, line 59 to col. 3, line 20 and **FIG. 3**); forming a metal coating **(FIG. 14: 31)** on the surface of the half-etched metal layer which is not covered by the photoresist wherein the metal coating comprises a layer of nickel covering the surface of the metal layer which is not covered by the photoresist, and a layer of metal selected from the group consisted of gold and palladium covering the nickel layer (col. 3, lines 2-6); stripping the photoresist within the cavities **(FIG. 14)**; etching the half-etched metal layer using the metal coating as a mask (col. 5, line 56 to col. 6, line 13 and **FIG. 14)** so as to form a plurality of connection pads **(FIG. 14: 142)** having a "substantially" concave profile (col. 5, line 66 to col. 6, line 4 and **FIG. 14**); attaching a semiconductor chip **(FIG. 15: 144)** onto the die pad **(FIG. 16: 138)** on the sheet carrier (col. 6, lines 14-15); electrically coupling the semiconductor chip to the connection pads (col. 6, lines 15-19); forming a package body **(FIG. 16: 148)** over the semiconductor chip and the connection pads wherein the substantially concave profile helps to lock the connection pads in the package body (col. 6, lines 21-26); removing the sheet carrier after the package body is formed (col. 6, lines 28-38 and **FIG. 17**); and forming a protective metal flash **(FIG. 17: 152)** on the lower surface of the connection pads exposed from the package body (col. 6, lines 28-38).

In re claims 5 and 22, **Coffman** does not explicitly disclose wherein the sheet carrier is completely removed from the package body in the step of removing the sheet carrier.

Yoneda discloses a method of making a low-pin-count chip package comprising the steps of: providing a sheet carrier **(FIG. 128: 320)**; attaching a semiconductor chip **(FIG. 128: 311)** onto the sheet carrier; electrically coupling the semiconductor chip to the connection pads **(FIG. 128: 315c)**; forming a package body **(FIG. 129: 314)** over the semiconductor chip and the connection pads; and removing the sheet carrier after the package body is formed, wherein the sheet carrier is completely removed from the package body in the step of removing the sheet carrier (page 22, paragraph [0460]-0469] and **FIGS. 128-131**) so that to expose a lower surface of the chip **(FIG. 131)**. It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Coffman and Yoneda to enable the sheet carrier of Coffman to be removed completely and furthermore the semiconductor devices can be fabricated and tested efficiently (page 1, paragraph [0011]).

In re claim 21, **Coffman** discloses wherein each of the connection pads having undercut areas **(FIG. 14: 142)** has an upper surface and a side wall extending downwardly from the upper surface, and the metal coating **(FIG. 14: 31 and 33)** is formed on the upper surface to cover not only the upper surface but also a portion of the side wall adjacent to the upper surface (col. 5, line 56 to col. 6, line 13 and **FIG. 14**).

In re claim 23, **Coffman** discloses wherein the step of removing the sheet carrier is performed before the step of forming the protective metal flash **(FIGS. 14-17)**.

2. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coffman (U.S. Patent 6,451,627) view of Yoneda et al. (U.S. Pub. 2002/0027265) as applied to claims 5,

6, 9, and 21-23 above, and further in view of Bernier et al. (U.S. Patent 6,251,707) and Bunyan (U.S. Pub. 2002/0012762).

In re claim 7, **Coffman** does not explicitly disclose wherein the sheet carrier is a polyimide tape with a layer of silicone adhesive.

Bernier disclose wherein the sheet carrier is a polyimide tape with a layer of silicone adhesive (col. 2, lines 30-41). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Coffman and Bernier to enable the sheet carrier of Coffman to be formed and furthermore to increase the heat conduction from the chip and thus minimize chip temperature (col. 2, lines 40-41).

In re claim 8, Neither **Coffman** nor **Bernier** discloses wherein the sheet carrier is a polyester tape with a layer of silicone adhesive.

Bunyan discloses wherein the sheet carrier is a polyester tape with a layer of silicone adhesive (page 3, paragraph [0034]). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Coffman and Bunyan to enable the sheet carrier of Coffman to be formed.

3. Claims 14, 15, 18, and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coffman (U.S. Patent 6,451,627) in view of Yoneda et al. (U.S. Pub. 2002/0027265).

In re claim 14, 15, and 18, **Coffman** disclose a method of making a low-pin-count chip package, the method comprising the steps of (**FIGS. 1-17** and related text): providing a sheet carrier **(FIG. 12: 126)**; laminating a metal layer **(FIG. 12: 124)** on the

sheet carrier; half-etching the metal layer so as to form cavities **(FIG. 14: 142)** at the predetermined positions thereof (col. 5, line 56 to col. 6, line 13 and **FIG. 14**); forming a photoresist layer **(FIG. 3: 32)** on the half-etched metal layer (col. 2, line 59 to col. 3, line 20); half-removing the photoresist layer such that only the photoresist within the cavities is left (col. 2, line 59 to col. 3, line 20 and **FIG. 3**); forming a metal coating **(FIG. 14: 31)** on the surface of the half-etched metal layer which is not covered by the photoresist wherein the metal coating comprises a layer of nickel covering the surface of the metal layer which is not covered by the photoresist, and a layer of metal selected from the group consisted of gold and palladium covering the nickel layer (col. 3, lines 2-6); stripping the photoresist within the cavities **(FIG. 14)**; etching the half-etched metal layer using the metal coating as a mask (col. 5, line 56 to col. 6, line 13 and **FIG. 14**) so as to form a die pad and a plurality of connection pads **(FIG. 14: 142)** having a "substantially" concave profile (col. 5, line 66 to col. 6, line 4 and **FIG. 14**); attaching a semiconductor chip **(FIG. 15: 144)** onto the die pad **(FIG. 16: 138)** on the sheet carrier (col. 6, lines 14-15); electrically coupling the semiconductor chip to the connection pads (col. 6, lines 15-19); forming a package body **(FIG. 16: 148)** over the semiconductor chip and the connection pads wherein the substantially concave profile helps to lock the connection pads in the package body (col. 6, lines 21-26); removing the sheet carrier after the package body is formed (col. 6, lines 28-38 and **FIG. 17**); and forming a protective metal flash **(FIG. 17: 152)** on the lower surface of the connection pads exposed from the package body (col. 6, lines 28-38).

In re claims 14 and 25, **Coffman** does not explicitly disclose wherein the sheet carrier is completely removed from the package body in the step of removing the sheet carrier.

Yoneda discloses a method of making a low-pin-count chip package comprising the steps of: providing a sheet carrier **(FIG. 128: 320)**; attaching a semiconductor chip **(FIG. 128: 311)** onto the sheet carrier; electrically coupling the semiconductor chip to the connection pads **(FIG. 128: 315c)**; forming a package body **(FIG. 129: 314)** over the semiconductor chip and the connection pads; and removing the sheet carrier after the package body is formed, wherein the sheet carrier is completely removed from the package body in the step of removing the sheet carrier (page 22, paragraph [0460]-0469] and **FIGS. 128-131**) so that to expose a lower surface of the chip **(FIG. 131)**. It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Coffman and Yoneda to enable the sheet carrier of Coffman to be removed completely and furthermore the semiconductor devices can be fabricated and tested efficiently (page 1, paragraph [0011]).

In re claim 24, **Coffman** discloses wherein each of the connection pads having undercut areas (FIG. 14: 142) has an upper surface and a side wall extending downwardly from the upper surface, and the metal coating **(FIG. 14: 31 and 33)** is formed on the upper surface to cover not only the upper surface but also a portion of the side wall adjacent to the upper surface (col. 5, line 56 to col. 6, line 13 and FIG. 14).

In re claim 25, **Coffman** discloses wherein the step of removing the sheet carrier is performed before the step of forming the protective metal flash **(FIGS. 14-17)**.

4. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coffman (U.S. Patent 6,451,627) view of Yoneda et al. (U.S. Pub. 2002/0027265) as applied to claims 14, 15, 18, and 24-25 above, and further in view of Bernier et al. (U.S. Patent 6,251,707) and Bunyan (U.S. Pub. 2002/0012762).

In re claim 16, **Coffman** does not explicitly disclose wherein the sheet carrier is a polyimide tape with a layer of silicone adhesive.

Bernier disclose wherein the sheet carrier is a polyimide tape with a layer of silicone adhesive (col. 2, lines 30-41). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Coffman and Bernier to enable the sheet carrier of Coffman to be formed and furthermore to increase the heat conduction from the chip and thus minimize chip temperature (col. 2, lines 40-41).

In re claim 17, Neither **Coffman** nor **Bernier** discloses wherein the sheet carrier is a polyester tape with a layer of silicone adhesive.

Bunyan discloses wherein the sheet carrier is a polyester tape with a layer of silicone adhesive (page 3, paragraph [0034]). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Coffman and Bunyan to enable the sheet carrier of Coffman to be formed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
April 9, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER